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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/023,127	12/17/2001	Joseph Williams	2	4580

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EXAMINER	
ROBERTS, BRIAN S	

ART UNIT	PAPER NUMBER
2662	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/023,127	WILLIAMS, JOSEPH	
	Examiner	Art Unit	
	Brian Roberts	2662	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12 and 14-25* is/are rejected.

7)☒ Claim(s) *13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *3/08/2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-25 have been examined.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 2, 10, 15, 17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

- In reference to claims 2, 10, 15, 17

The term "substantially" in claim 2, 10, 15, and 17 is a relative term which renders the claim indefinite. The term " substantially" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-11 and 15-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Carvey et al. (US 6934471) in view of Flanagan et al. (US 5159595)

- In reference to claim 1, 16, 23

Carvey et al. teaches a switching system and method that includes:

- In Figure 2, a receiver (102) for receiving packets
- In Figure 3, a transmitter (103) for transmitting packets
- In Figure 2, a input Time-Slot Interchanger (111) coupled to the first half-duplex link (101) and to the receiver (102) configurable to reorder the data packets received from the receiver (102) (column 3 lines 29-32)
- In Figure 3, a output Time-Slot Interchanger (111) coupled to the second half-duplex link (107) and to the transmitter (106) configurable to reorder the data packets to be transmitted by the transmitter (106) (column 5 lines 62-63)

Carvey et al. does not explicitly teach a controller coupled to the receiver and transmitter where the controller is configured to route the packets to an output of the cross-connect switch or an adjacent or node in the mesh architecture.

In Figure 5, Flanagan et al. teaches anode in a synchronous optical network that includes a control processor 58 that is coupled to a receiver (18) and transmitter (20) an configured to route packets to adjacent nodes as shown in Figure 6.

It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the system and method of Carvey et al. to include a control processor coupled to the receiver and transmitter where the controller is configured to route the packets to adjacent nodes as taught by Flanagan et al. because it allows

packets to be routed from a source node to a destination node via a plurality of nodes in a network, such as in a synchronous optical network, and the packets can be routed through nodes configured in a ring topology.

- In reference to claim 2, 17, as best understood

The combination of Carvey et al. and Flanagan et al. teach a system and method that covers substantially all limitations of the parent claim. Carvey et al. further teaches routing the packets in a conflict-free manner.

- In reference to claim 3, 18, 25

The combination of Carvey et al. and Flanagan et al. teach a system and method that covers substantially all limitations of the parent claim. In Figure 9, Carvey et al. further teaches the Time-Slot Interchanger (111) including a circular buffer (routing buffer) in memory (221) (column 4 lines 45-48) to store the packets during reordering of the packets.

- In reference to claim 4, 19, 24

The combination of Carvey et al. and Flanagan et al. teach a system and method that covers substantially all limitations of the parent claim.

Carvey et al. does not teach a connection map coupled to the controller, where the controller routes the packet in accordance with information stored in the connection map.

In Figure 5, Flanagan et al. teaches the control processor (58) maintains a connection map used to set us the TSIs and selectors within the node to provide the desired routing of each STS-1 signal. (column 9 lines 12-17)

It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the system and method of Carvey et al. to include a connection map coupled to the controller, where the controller routes the packet in accordance with information stored in the connection map as taught by Flanagan et al. because it allows packets to be routed from a source node to a destination node via a plurality of nodes in a network, such as in a synchronous optical network, and the packets can be routed through nodes configured in a ring topology.

- In reference to claim 5-7, 20-21

The combination of Carvey et al. and Flanagan et al. teaches a system and method that covers substantially all limitations of the parent claim. In Figures 1-3, Carvey et al. further teach that the receiver (102) and transmitter (106) inherently contain a serializer/deserializer that convert a 16-bit wide stream into a serial stream/serial stream into a 16-bit wide stream (column 1 lines 20-28) and a input/output interface. The receiver and transmitter in the node form a transceiver.

- In reference to claim 8, 22

The combination of Carvey et al. and Flanagan et al. teaches a system and method that covers substantially all limitations of the parent claim. Carvey et al. further teaches:

- In Figure 4 and 5, a predefined sequence that reduces routing the packets in the mesh architecture from four possible connections when the packet first arrives at the node to one-to-one routing within each time slot as shown in Figure 5 (column 3-4 lines 61-5)
- The interchangers, knowing the pattern in advance, schedules (reorder) packets to appear on a which input switch during the time period when that input is connected to the desired output (column 4 lines 5-10)
- Routing packets from a source (113) to a destination (107)

Carvey does not explicitly teach a system with a plurality of nodes or reordering the packets with the destination node.

Flanagan et al. teaches a controller inherently containing a processor, and routing data packets from a source node to a destination node.

It would have been obvious to a person of ordinary skill in the art at the time of the invention to implement the photonic switch and method of Carvey et al. in a system with a plurality of nodes where the nodes, each node comprise a controller inherently containing a processor, as taught by Flanagan et al. because it allows the packets to be routed from a source node to a destination node via a plurality of nodes in a network, such as in a synchronous optical network, and the packets can be routed through nodes configured in a ring topology.

- In reference to claim 9

Carvey et al. teaches a switching system and method that includes:

- In Figure 4 and 5, a predefined sequence that reduces routing the packets in the mesh architecture from four possible connections when the packet first arrives at the node to one-to-one routing within each time slot as shown in Figure 5 (column 3-4 lines 61-5)
- The interchangers, knowing the pattern in advance, schedules (reorder) packets to appear on a which input switch during the time period when that input is connected to the desired output (column 4 lines 5-10)
- Routing packets from a source (113) to a destination (107)

Carvey does not explicitly teach a system with a plurality of nodes or reordering the packets with the destination node.

Flanagan et al. teaches a controller inherently containing a processor, and routing data packets from a source node to a destination node.

It would have been obvious to a person of ordinary skill in the art at the time of the invention to implement the photonic switch and method of Carvey et al. in a system with a plurality of nodes where the nodes, each node comprise a controller inherently containing a processor, as taught by Flanagan et al. because it allows the packets to be routed from a source node to a destination node via a plurality of nodes in a network, such as in a synchronous optical network, and the packets can be routed through nodes configured in a ring topology.

- In reference to claim 10, as best understood

The combination of Carvey et al. and Flanagan et al. teach a system and method that covers substantially all limitations of the parent claim. Carvey et al. further teaches routing the packets in a conflict-free manner.

- In reference to claim 11

The combination of Carvey et al. and Flanagan et al. teach a system and method that covers substantially all limitations of the parent claim. In Figure 9, Carvey et al. further teaches the Time-Slot Interchanger (111) including a circular buffer in memory (221) (column 4 lines 45-48) to store the packets before they are forwarded through the switch to the destination.

- In reference to claim 15, as best understood

The combination of Carvey et al. and Flanagan et al. teach a system and method that covers substantially all limitations of the parent claim. In Figures 4-7, Carvey et al. further teaches partitioning time-slots into a plurality of segments associated with the plurality of nodes. Carvey et al. further teaches routing the data samples from the source to a destination and reordering the data samples in a parallel within each of the plurality of segments. (column 3-4 lines 61-12)

Claims 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Carvey et al. (US 6934471) in view of Flanagan et al. (US 5159595), as applied to the parent claim, and further in view of Zheng.

- In reference to claim 12

The combination of Carvey et al. and Flanagan et al. teach a system and method that covers substantially all limitations of the parent claim.

The combination of Carvey et al. and Flanagan et al. does not teach performing systolic sorting on the data.

Zheng et al. teaches a systolic sorting system and method.

It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Carvey et al. and Flanagan et al. to include performing systolic sorting on the data because it is feasible for VLSI implementation and its time performance is virtually independent of the cost and depth of the underlying sorting network.

Claims 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Carvey et al. (US 6934471) in view of Flanagan et al. (US 5159595), as applied to the parent claim, and further in view of Carpinelli et al.

- In reference to claim 14

The combination of Carvey et al. and Flanagan et al. teach a system and method that covers substantially all limitations of the parent claim.

The combination of Carvey et al. and Flanagan et al. does not teach computing a graph-theoretic model for the routing sequences.

Carpinelli et al. teaches computing a graph-theoretic model for routing in parallel computers.

It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Carvey et al. and Flanagan et al. to include computing a graph-theoretic model for routing in parallel computers as taught by Carpinelli et al. because it would improve the efficiency of a complex optical switching system.

Allowable Subject Matter

Claim 13 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter because the prior record fails to teach or fairly suggest precomputing one or more routing sequences, the routing sequences reducing a routing in the mesh to a one-to-one routing within each of the time-slots; reordering the data samples within one or more source nodes in accordance with the precomputed routing sequences, routing the data samples from the one or more corresponding destination nodes through the mesh arrangement; and source nodes to one or more reordering the data samples within the destination nodes, whereby the data samples are transmitted during a

connect time-slot; routing the data samples in a first dimension in parallel in accordance with the precomputed routing sequences to determine corresponding destination nodes; routing the data samples in a second dimension in parallel, whereby the data samples are routed to intended nodes in the first dimension, and routing the data samples in the first dimension in parallel whereby each of the data samples are routed to the corresponding destination nodes.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure are:

- Rezai et al. (US 6584119) teaches a dialable data services/TDM bandwidth management.
- Shiragaki (US 5457556) teaches an optical cross-connect system with space and wavelength division multiplexing.
- Wu et al. (US 2003/0021267) teaches a non-blocking grooming switch.
- Dally (US 6870838) teaches a multistage digital cross connect with integral frame timing
- Notani (US 6850660) teaches a SONET/SDH transmission apparatus and method.
- Elliot et al. (US 6587470) teaches flexible cross-connect with data plane.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian Roberts whose telephone number is (571) 272-3095.. The examiner can normally be reached on M-F 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou can be reached on (571) 272-3088. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

BSR
09/16/2005

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